“Design of Multi-Gigabit ATCA Backplanes and Logic Card Interfaces"
An ATCA Summit Presentation


Development Based on the Work of
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Presented by
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NESA Overview

- Founded in 1973, NESA helps start-ups and established companies get to market quickly with superior products. NESA is in the business of reducing the risks of integrating advanced technology and increasing a client’s return on investment.

- NESA provides design and analysis of high performance products for networking, telecommunications, computer, semiconductor and interconnect companies.

**NESA is “Right by Design” - Design Expertise & Maturity**

**NESA Means Time to Market with Competitive Products**

**NESA is an Experienced Gigabit Technology Partner**

**NESA is an ATCA Technology Gateway and Solution Provider**
The design and qualification of multi-Gigabit ATCA and MicroTCA backplanes is a complex process. As the ATCA specification is presently written, the interconnects are defined in terms of the logical slot numbering, which permits various physical configurations. The two architectures supported by the ATCA specification are single or redundant switch centric and full or partial meshes.

This tutorial will focus on the interconnect design of various ATCA backplane architectures. For simplicity, switch architectures will be emphasized but the principles will apply to mesh architectures as well. Topics will cover:

- Various differential architectures
- The limits of FR-4 with respect to data rates,
- A review of background technology to assist in designing with low loss dielectric materials,
- What differential impedance means and how to design traces to meet the 100 Ω fabric and 130 Ω clock differential trace requirements.

Fabric speeds in excess of 1.25 Gbps will be the major focus.
Introduction to ATCA Architectures

- The ATCA system interconnect architecture specification has been written in terms of logical slot connections. The designer is then free to map the logical architecture onto the physical architecture of chassis and backplane. Different combinations of logical and physical locations lead to dramatically different architectures.

- The most popular configurations are the centralized 14-slot switch and 5-slot full mesh architectures. Other architectures which have been seen are non-centralized redundant switches.

- The latter is more difficult to rout but provides redundancy with respect to the cooling system; that is, if a fan fails over one of the switches, the other switch remain in operation. When switch locations are left and right justified, the traces tend to be longer and suffer more loss between the switch and node cards.
Centralized Switch Architecture Features

- Shortest overall trace lengths: Improved FR-4 usable to perhaps 5 Gbps.
- Simplest and least expensive to layout & rout.
- Three thermal zones: Use six (6) 5 ¼” high capacity fans to cover the area. An N+1 reliability cooling design probably not possible.
- Single point of thermal failure with highest power boards.
- Unbalanced thermal zones and potential for maximum flow choke.
- Probably will be the most common design for all time!
Enhanced Thermal Reliability Dual Star Architecture

Data Fabric

Low Power Cooling Zone #1  High Power Cooling Zone #2  High Power Cooling Zone #3  Low Power Cooling Zone #4
Separated Switch Architecture Features

- Medium overall trace lengths: Improved FR-4 usable to perhaps 5 Gbps.
- Somewhat more complex to layout & rout.
- No single point of thermal failure with highest power boards.
- Perhaps four (4) independent thermal zones rather than three (3). Smaller diameter high capacity fans provide a measure of redundancy for N+1 reliable designs. Might raise the cost of fan tray solutions.
- Balanced thermal zones and low potential for flow choke.
- Uncommon physical architecture in Telecom industry.
Isolated Switch Architecture
Isolated Switch Architecture Features

- Longest overall trace lengths: Improved FR-4 usable to perhaps 3.125 Gbps.
- Complex to layout & rout and requires higher layer count due to crossovers.
- No single point of thermal failure with highest power boards.
- Perhaps three (3) independent thermal zones rather than four (4).
- Balanced thermal zones and low potential for maximum flow choke.
- Common physical architecture in Telecom industry.
Practical ATCA Backplane Design Features

- Backplane material choices and design impacts
- Differential Impedance
- Bussed clocks
- Data Fabric Requirements and Characteristics
- Performance and technology roadmap
### Selected Properties of PWB Materials

<table>
<thead>
<tr>
<th>PWB Material</th>
<th>Dielectric Constant</th>
<th>Measured Conditions</th>
<th>Dissipation Factor @ 1 mT</th>
<th>CTE(^2) (PPM/°C)</th>
<th>Tensile Modulus (MPSI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTFE</td>
<td>2.14</td>
<td>@ 10 GHz</td>
<td>0.0004</td>
<td>224</td>
<td>224</td>
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<tr>
<td>PTFE/Microfiber</td>
<td>2.20</td>
<td>@ 10 GHz</td>
<td>0.0008</td>
<td>24</td>
<td>261</td>
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<td>RO-3003</td>
<td>3.00</td>
<td>@ 10 GHz</td>
<td>0.0013</td>
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<tr>
<td>RO4403</td>
<td>3.17</td>
<td>@ 10 GHz</td>
<td>0.005</td>
<td>16 - 19</td>
<td>80</td>
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<tr>
<td>Nelco 6000-SI</td>
<td>3.20</td>
<td>@ 2.5 Ghz</td>
<td>TBD</td>
<td>9 - 13</td>
<td>3.70%</td>
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<tr>
<td>Polyimide / Quartz</td>
<td>3.35</td>
<td>@ 1 MHz</td>
<td>0.005</td>
<td>6-8</td>
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<td>RO4003</td>
<td>3.38</td>
<td>@ 10 GHz</td>
<td>0.0027</td>
<td>11 - 14</td>
<td>46</td>
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<td>Nelco 6000</td>
<td>3.40</td>
<td>@ 2.5 Ghz</td>
<td>0.009</td>
<td>10 - 12</td>
<td>3.70%</td>
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<td>RO4350B</td>
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<td>0.004</td>
<td>14 - 16</td>
<td>50</td>
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<td>RO4450B</td>
<td>3.54</td>
<td>@ 10 GHz</td>
<td>0.004</td>
<td>16 - 19</td>
<td>60</td>
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<td>Polyimide / Kevlar</td>
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<td>@ 1 MHz</td>
<td>0.008</td>
<td>3.4-6.7</td>
<td>83</td>
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<tr>
<td>Nelco 4000-13</td>
<td>3.70</td>
<td>@ 2.5 Ghz</td>
<td>0.014</td>
<td>10 - 14</td>
<td>3.50%</td>
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<tr>
<td>Nelco 4000-6</td>
<td>4.1</td>
<td>@ 2.5 Ghz</td>
<td>0.022</td>
<td>12 - 16</td>
<td>3.90%</td>
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<tr>
<td>Polyimide / Glass</td>
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<td>0.01</td>
<td>11.7-14.2</td>
<td>60</td>
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<tr>
<td>Epoxy / Glass</td>
<td>4.80</td>
<td>@ 1 MHz</td>
<td>0.022</td>
<td>12.8-16</td>
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From: "Fluoropolymer Composite PWB for High Speed Digital Applications"
Orlando, FL

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Stripline Impedance vs. Trace Width and Height
Trace - to Plane (Plane to Plane = 2H)
FR-4 and 0.5 oz. Copper

<table>
<thead>
<tr>
<th>Stripline Impedance (ohms)</th>
<th>Trace Width (mils)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 Ω solutions</td>
<td></td>
</tr>
<tr>
<td>75 Ω solutions</td>
<td></td>
</tr>
<tr>
<td>60 Ω solutions</td>
<td></td>
</tr>
<tr>
<td>50 Ω solutions</td>
<td></td>
</tr>
<tr>
<td>65 Ω Solutions</td>
<td></td>
</tr>
</tbody>
</table>

- 3.0
- 4.0
- 5.0
- 6.0
- 7.0
- 8.0
- 9.0
- 10.0
- 12.5
- 15.0
- 20.0
- 30.0

Height - H

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FR-4 Insertion Loss (dB) per meter

DC Loss = Skin Effect Loss @ 70.65 MHz, Skin Loss = Dielectric Loss @ 330.56 MHz

Differential FR-4 PCB: DC, Cu Skin Effect, Dielectric and Total Loss vs. Frequency
(Trace Impedance = 100 ohms, Avg. trace width ~ 6.2mils [0.158mm], 0.5 Oz Copper)

Note: 10 dB/m = 0.254 dB/in = 3.05 dB/ft
Nelco-4000-13SI Insertion Loss (dB) per meter

DC Loss = Skin Effect Loss @ 66.6 MHz, Skin Effect Loss = Dielectric Loss @ 1474 MHz

Note: 10 dB/m = 0.254 dB/in = 3.05 dB/ft
ATCA Bussed Synchronization Clock
Design Summary
Typical ATCA Dual Star Switch Backplane - CLK Area

- CLK Area
- Redundant Switches
- Node Cards
- Data Fabric Area
- Base Fabric Area
- Redundant –48 VDC Primary Power
- Blade Power Connectors
- Redundant –48 VDC Primary Power
- Fans, IPMI, etc.
Working Impedance of Bussed Clock Traces

Vias, connectors and trace stubs have a MAJOR affect on the working controlled impedance of a printed wiring logic board and backplane. To a good approximation, the following equation permits the evaluation of via, connector and stub effects:

\[ Z_{\text{working}} = Z_o \sqrt{\frac{1}{1 + \frac{N^*C_L}{\ell^*C_o}}} \]

where:

- \( Z_o \) is the raw etch transmission line impedance, and
- \( L_o \) and \( C_o \) are the raw etch per unit inductance [nH/m, nH/in, etc.] and capacitance [pf/m, pf/in, etc.]
- \( N \) = number of capacitive loads,
- \( C_L \) = total capacitance per load [pf, nf, etc.]
ATCA Bussed Synchronism Clock Impedance

- Clock bus impedance measurements should take place at either end of the bus in a clock termination location after the termination resistor is removed.

- The raw etch differential design impedance of the bussed M-LVDS ATCA clock interfaces on the backplane should be $130 \, \Omega \pm 10\%$.

- The connector via capacitance taken together over each slot lowers the raw etch impedance from $130 \, \Omega$ to about $105 \, \Omega$.

- When the ZD connectors are pressed into the backplane, their bussed capacitive loading will lower the impedance to about $100 \, \Omega$. This is called the un-filled bus slot impedance.

- The $80.6 \, \Omega$ termination resistors at each end of the bus is a compromise value between the un-filled slot impedance of $\sim 100 \, \Omega$ and the filled slot impedance $\sim 60 \, \Omega$. 
ATCA SI Measurement Set-ups

TDR/TDT/Skew Set-up

- HP54750A with HP54754A & HP54751A plug-ins
- NESA differential probes on bare backplane

Eye Pattern Set-up

- Advantest D3186 PPG driving HP54751A plug-in in Agilent Infinium DCA 86100A Oscilloscope
- NESA test probe cards in backplane with headers
Measurement of Bussed Clocks Trace Impedance,
(Drilled and Plated Vias, No Connectors)

Synchronization Clocks (M-LVDS): TDR Impedance Comparison
Bare Backplane (PTHs only) - "Live" Trise~35ps at TDR Gen.

Via Loading Effects ~ 26 Ω

Raw Etch Impedance = 130 Ω
Measurement of Bussed Clocks Trace Impedance, (Drilled and Plated Vias and Connectors)

Synchronization Clocks (M-LVDS): TDR Impedance Comparison
Backplane with HM-ZD connector headers - "Live" Trise~35ps at TDR Gen.

- Raw Etch Impedance ~ 130Ω
- Via and bkpln connector loading ~ 29Ω
- Impedance: start ~ 101Ω, average ~ 103Ω over length to 80.6Ω termination

Probe inserted at first PTH
Test cables/probe
Probe inductance
ATCA Bussed Clock Design Summary

- The drilled vias for the ZD connector have, by far, the most significant effect on the ATCA clock bus impedance and lower the effective impedance by approximately (26 – 30) Ω.

- The effect of the backplane half of the connector is small. Where there are unpopulated slots, the ATCA clock bus impedance will be ~ 100 Ω.

- Although not shown, the “working differential impedance” of a full populated ATCA clock bus is ~ 60 Ω provided the stub length maximum is observed on the switch and node blades.

- The M-LVDS clock drivers “see” the bus differential impedance to be ~ 30 Ω. M-LVDS drivers are capable of driving this low impedance bus to full swing voltage due to their ample current drive capabilities. LVDS clock drivers do not have sufficient drive capabilities.
Fabric, Base and Update Channel
Impedance, Skew, Insertion Loss and Xtalk
Requirements
Fabric, Base and Update Channel Impedance, Skew, Insertion Loss and Xtalk Requirements

- ATCA Backplane and Blade serial Fabric, Base, and Update Channel Link differential impedance of the is $100 \, \Omega \pm 10\%$.
- Fabric and Base Interface skew requirements:
  - Fabric Interface: The transmit and receive pairs within a channel should each have a matched delay of better than 17 ps.
  - Base Interface: All four pairs within a channel shall have a matched delay of better than 60 ps.
  - Skew within any differential pair shall not exceed 3.4 ps.
- Insertion loss should follow the limits as specified up to 5 GHz (10 Gbps).
- The near-end differential crosstalk (NEXT) coefficient should be $< 0.2\%$ for 35 mil spaced edge-coupled FR-4 designs. Results for other materials may vary but will be small.
Sample Fabric Interface Pair Measurements

- **TDR** – Impedance for both Transmit and Receive paths
  - Channel 1  \(Tx[3:0]\) and \(Rx[3:0]\) – Pass, Pass
  - Channel 15 \(Tx[3:0]\) and \(Rx[3:0]\) – Pass, Pass

- **Time Domain Transmission (TDT)** Propagation Delay, Skew and Losses (Risetime and Amplitude)
  - Channel 1  \(Tx[3:0]\) and \(Rx[3:0]\) – Pass, Pass
  - Channel 15 \(Tx[3:0]\) and \(Rx[3:0]\) – Pass, Fail

- **Eye-diagram Response @ 3.125, 5.00 and 6.25 Gbps**
  - Eye Width and Eye Height – Pass, Pass, Fail
  - Jitter (p-p), Jitter (RMS) – Pass, Pass, Fail
Typical ATCA Dual Star Switch Backplane: Fabric Area

- CLK Area
- Data Fabric Area
- Base Fabric Area
- Redundant Switches
- Node Cards
- Redundant –48 VDC Primary Power
- Blade Power Connectors
- Redundant –48 VDC Primary Power
- Fans, IPMI, etc.
Sample Fabric Interface Pair Measurements

TDR – Impedance
Fabric Interface: Ch.1 Tx Pair TDRs
"live" Trise ~35ps at TDR generator

Probe Fixture Effect
Design of Multi-Gigabit ATCA Backplanes

Fabric Interface: Ch.1 Rx Pair TDRs
"Live" Trise ~35ps at TDR generator

Probes Fixture Effect
Fabric Interface: Ch.15 Tx Pair TDRs
"Live" Trise ~35ps at TDR generator

Probe Fixture Effect
Fabric Interface: Ch.15 Rx Pair TDRs
"live" Trise ~35ps at TDR generator

Probe Fixture Effect
Sample Fabric Interface Pairs

Time Domain Transmission – Prop. Delay, Skew, and Losses
Differential Transmission Measurements

Four Transmit Pairs (Ch. 1)

<table>
<thead>
<tr>
<th>Pair</th>
<th>Gain (%)</th>
<th>Trise,out (ps)</th>
<th>Prop. Delay* (ns)</th>
<th>Max. Skew (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX0</td>
<td>97.1</td>
<td>363</td>
<td>2.814</td>
<td></td>
</tr>
<tr>
<td>TX1</td>
<td>97.1</td>
<td>368</td>
<td>2.824</td>
<td></td>
</tr>
<tr>
<td>TX2</td>
<td>97.1</td>
<td>353</td>
<td>2.806</td>
<td></td>
</tr>
<tr>
<td>TX3</td>
<td>97.1</td>
<td>375</td>
<td>2.824</td>
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</table>

Note: AdvancedTCA™ skew requirement between Fabric Transmit Pairs and between Receive Pairs is 17ps (0.017ns).

* Delays include NESA fixturing - these are relative measurements for determination of skew

Receive Pair DTDT Data

<table>
<thead>
<tr>
<th>Pair</th>
<th>Gain (%)</th>
<th>Trise,out (ps)</th>
<th>Prop. Delay* (ns)</th>
<th>Max. Skew (ns)</th>
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<tbody>
<tr>
<td>RX0</td>
<td>97.1</td>
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<td>RX1</td>
<td>97.1</td>
<td>376</td>
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<tr>
<td>RX2</td>
<td>97.1</td>
<td>382</td>
<td>2.753</td>
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<td>RX3</td>
<td>97.1</td>
<td>372</td>
<td>2.753</td>
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</table>

Note: AdvancedTCA™ skew requirement between Fabric Transmit Pairs and between Receive Pairs is 17ps (0.017ns).

* Delays include NESA fixturing - these are relative measurements for determination of skew
Differential Transmission Measurements

Four Transmit Pairs (Ch.15)

Four Receive Pairs (Ch.15)

<table>
<thead>
<tr>
<th>Transmit Pair DTDT Data</th>
<th>Pair</th>
<th>Gain (%)</th>
<th>Trise,out (ps)</th>
<th>Prop. Delay* (ns)</th>
<th>Max. Skew (ns)</th>
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<tbody>
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<td>TX3</td>
<td>96.7</td>
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<thead>
<tr>
<th>Receive Pair DTDT Data</th>
<th>Pair</th>
<th>Gain (%)</th>
<th>Trise,out (ps)</th>
<th>Prop. Delay* (ns)</th>
<th>Max. Skew (ns)</th>
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<tr>
<td>RX3</td>
<td>97.5</td>
<td>397</td>
<td>2.778</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: AdvancedTCA™ skew requirement between Fabric Transmit Pairs and between Receive Pairs is 17ps (0.017ns).

* Delays include NESA fixturing - these are relative measurements for determination of skew
Sample Fabric Interface Pairs

Receive Eye Patterns

PRBS $2^{23}-1$ at 3.125Gbps
Reference Eye Pattern
Data Rate = 3.125Gbps

Jitter (p-p) = 11ps
Jitter (RMS) = 2ps
Eye Width* = 302ps
Eye Height** = 972mV

Note: Rx mask per ATCA test plan;
Jitter = 0.25UI, amplitude +/- 100mV.
Mask slope not specified (XAUI less steep).

* Widest inside opening at zero-crossing
** Largest inside opening at center of eye
Fabric Interface: Sample Transmit & Receive Pairs

Data Rate = 3.125Gbps

Transmit Pair

Receive Pair

Jitter (p-p) = 57ps
Jitter (RMS) = 13ps
Eye Width* = 262ps
Eye Height** = 568mV

Note: Rx mask per ATCA test plan;
Jitter =0.25UI, amplitude +/-100mV.
Mask slope not specified (XAUt less steep).

* Widest inside opening at zero-crossing
** Largest inside opening at center of eye

Jitter (p-p) = 51ps
Jitter (RMS) = 11ps
Eye Width = 265ps
Eye Height = 548mV
Sample Base Interface Pairs

Receive Eye Patterns

PRBS $2^{23}-1$ at 3.125Gbps
Base Interface: Sample Transmit & Receive Pairs
Data Rate = 3.125Gbps

Transmit Pair

- Jitter (p-p) = 55ps
- Jitter (RMS) = 12ps
- Eye Width* = 260ps
- Eye Height** = 568mV

Receive Pair

- Jitter (p-p) = 57ps
- Jitter (RMS) = 11ps
- Eye Width = 262ps
- Eye Height = 552mV

Note: Rx mask per ATCA test plan;
Jitter =0.25UI, amplitude +/-100mV.
Mask slope not specified (XAUI less steep).

* Widest inside opening at zero-crossing
** Largest inside opening at center of eye
Sample Fabric Interface Pairs

Receive Eye Patterns

PRBS $2^{23} - 1$ at 5 Gbps and 6.25 Gbps
Fabric Interface: Reference Eye Patterns
Data Rate = 5 Gbps and 6.25 Gbps

5Gbps Reference

- Jitter (p-p) = 12ps
- Jitter (RMS) = 2ps
- Eye Width* = 186ps
- Eye Height** = 936mV

6.25Gbps Reference

- Jitter (p-p) = 11ps
- Jitter (RMS) = 2ps
- Eye Width = 145ps
- Eye Height = 932mV

Note: Rx mask per XAUI spec., scaled to specified data rates; amplitude +/-100mV.

* Widest inside opening at zero-crossing
** Largest inside opening at center of eye
Fabric Interface: Sample Pair Eye Patterns

Data Rate = 5 Gbps and 6.25 Gbps

Fabric Pair at 5Gbps

- Jitter (p-p) = 57ps
- Jitter (RMS) = 11ps
- Eye Width* = 140ps
- Eye Height** = 264mV

Fabric Pair at 6.25Gbps

- Jitter (p-p) = 81ps
- Jitter (RMS) = 14ps
- Eye Width = 80ps
- Eye Height = 128mV

Note: Rx mask per XAUI spec., scaled to specified data rates; amplitude +/-100mV.

* Widest inside opening at zero-crossing
** Largest inside opening at center of eye
Fabric Interface: Sample Pair Eye Patterns
Data Rate = 5Gbps and 6.25Gbps

Fabric Pair at 5Gbps

![Eye Pattern Image]

- Jitter (p-p) = 60ps
- Jitter (RMS) = 11ps
- Eye Width* = 141ps
- Eye Height** = 336mV

Note: Rx mask per XAUI spec., scaled to specified data rates; amplitude +/-100mV.

* Widest inside opening at zero-crossing
** Largest inside opening at center of eye

Fabric Pair at 6.25Gbps

![Eye Pattern Image]

- Jitter (p-p) = 66ps
- Jitter (RMS) = 13ps
- Eye Width = 97ps
- Eye Height = 200mV (no margin)
ATCA Backplane Design Summary

- The ATCA backplane specification permits a wide variety of physical implementations as shown in the presentation.
- The choice of PCB materials strongly determines the upper limit if data rate across the data fabric, although via fabrication technology can be very important.
- The ATCA bussed clock design permits redundant distribution of synchronism clocks and utilizes M-LVDS technology. Design of the bus must take into account the loading effects of the connector, vias and stubs.
- The ATCA data fabric has strict impedance and channel skew limits which must take into account the connector and trace effects. To exceed the minimum data rates, the ATCA specification guidelines must be extended to take into account material, trace, via and fabrication connector-via bandwidth limit mitigation.
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Many Thanks for your kind attention!